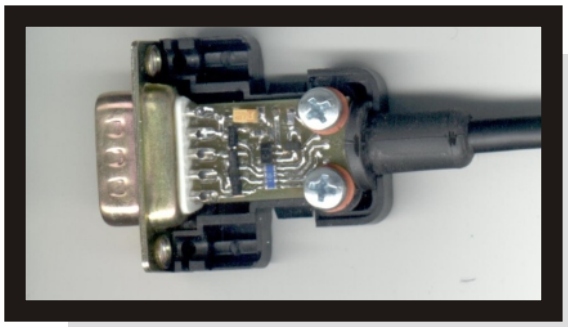
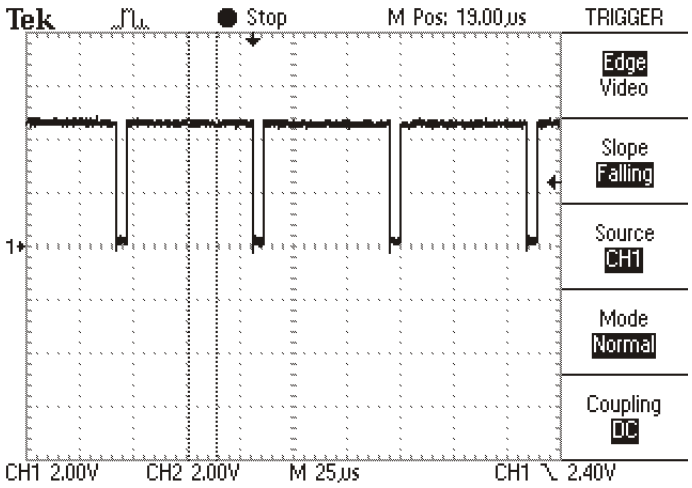
sinclair QL csync-inverter

The QL cannot be connected to a CGA monitor directly. This is because the QL has an active-low Csync pin. A CGA monitor expects an active-high signal. This document shows how to make a very little circuit board, which inverts the Csync pin. No additional power supply is needed. The PCB is small enough to fit inside a DB-9 connector.

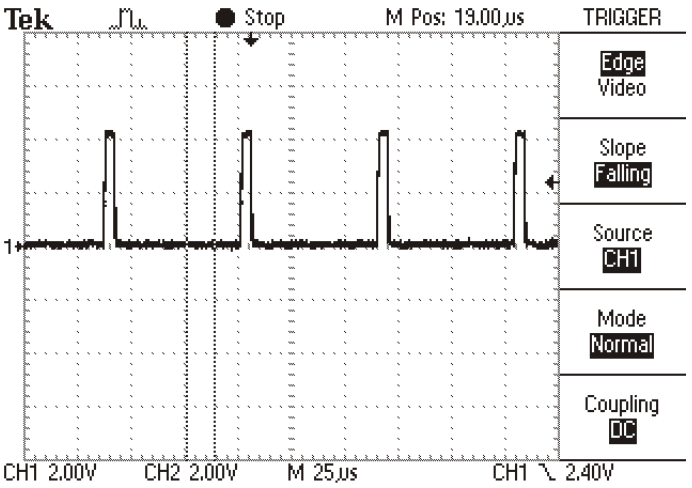


Here are some pictures of the cable.

The circuit is straightforward. The Csync signal is fed through a single gate NAND, which acts as the inverter. The NAND gate is powered by the Csync signal itself. Energy is stored in a 10uF tantalum capacitor, to buffer the time the Csync signal is low. A 100 ohm resistor is added to limit the inrush current during power-up. Some additional resistors and SOT-23 transient suppressors are added for extra protection of the QL.

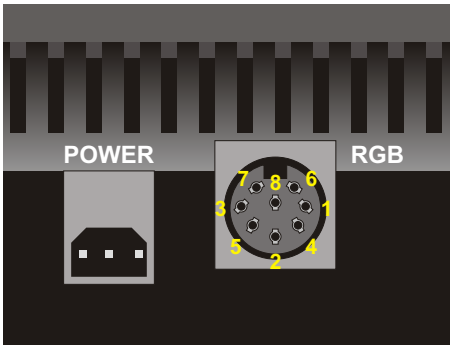


Here you can see the 'original' Csync signal, measured directly at the 8-pin DIN connector at the rear of the QL.



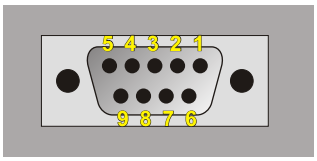
Inverted signal

QL monitor pinout



1	PAL	Composite PAL
2	GND	Ground
3	Video	Composite Mono Video
4	Csync	Composite Sync
5	Vsync	Vertical Sync
6	Green	Color Signal
7	Red	Color Signal
8	Blue	Color Signal

CGA DB-9 pinout



1	GND	Ground
2	GND	Ground
3	Red	Color Signal
4	Green	Color Signal
5	Blue	Color Signal
6	-	
7	-	
8	Hsync	(Inverter QL-Csync)
9	Vsync	Vertical sync

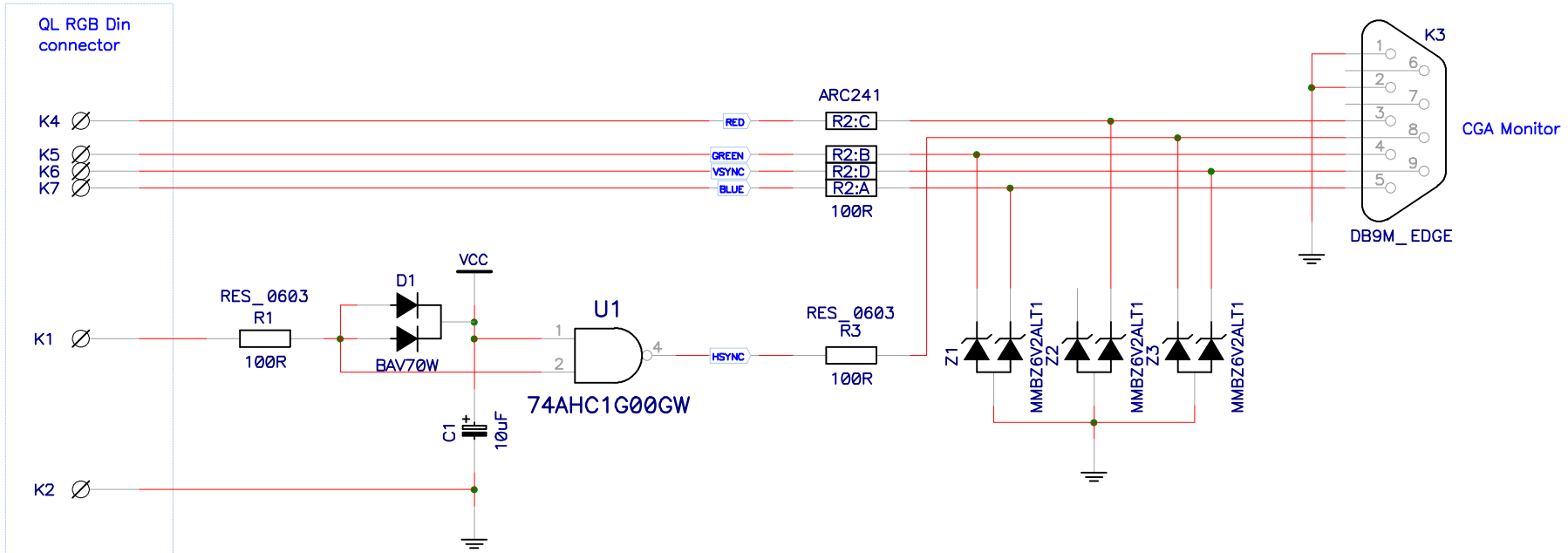
The schematic drawing is shown on the following page.
The following components are needed:

Qty	RefDes	Component	Value	Description	PatternName
1	U1	74AHC1G00GW		SingleGate NAND	SOT353
1	R2	ARC241	100R	Resistor Array	ARC241
1	D1	BAV70W		Dual Diode	SOT323
1	C1	CAP_SIZEA	10uF	Tantalum Cap.	SIZE_A
1	K3	DB9M_EDGE		SubD Connector	DB9EDGEM
3	Z1,Z2,Z3	MMBZ6V2ALT1	6.2V	Transient Abs.	SOT23
2	R1,R3	RES_0603	100R	Resistor	0603

Additional stuff:
6 core cable (screened if possible).
8 pin QL style DIN connector.
Sub-D hood. ADT09 from Assmann, www.assmann.com, see picture on first page.
2 Washers, which are below the two screws inside the sub-D hood. See picture.
The circuitboard itself.

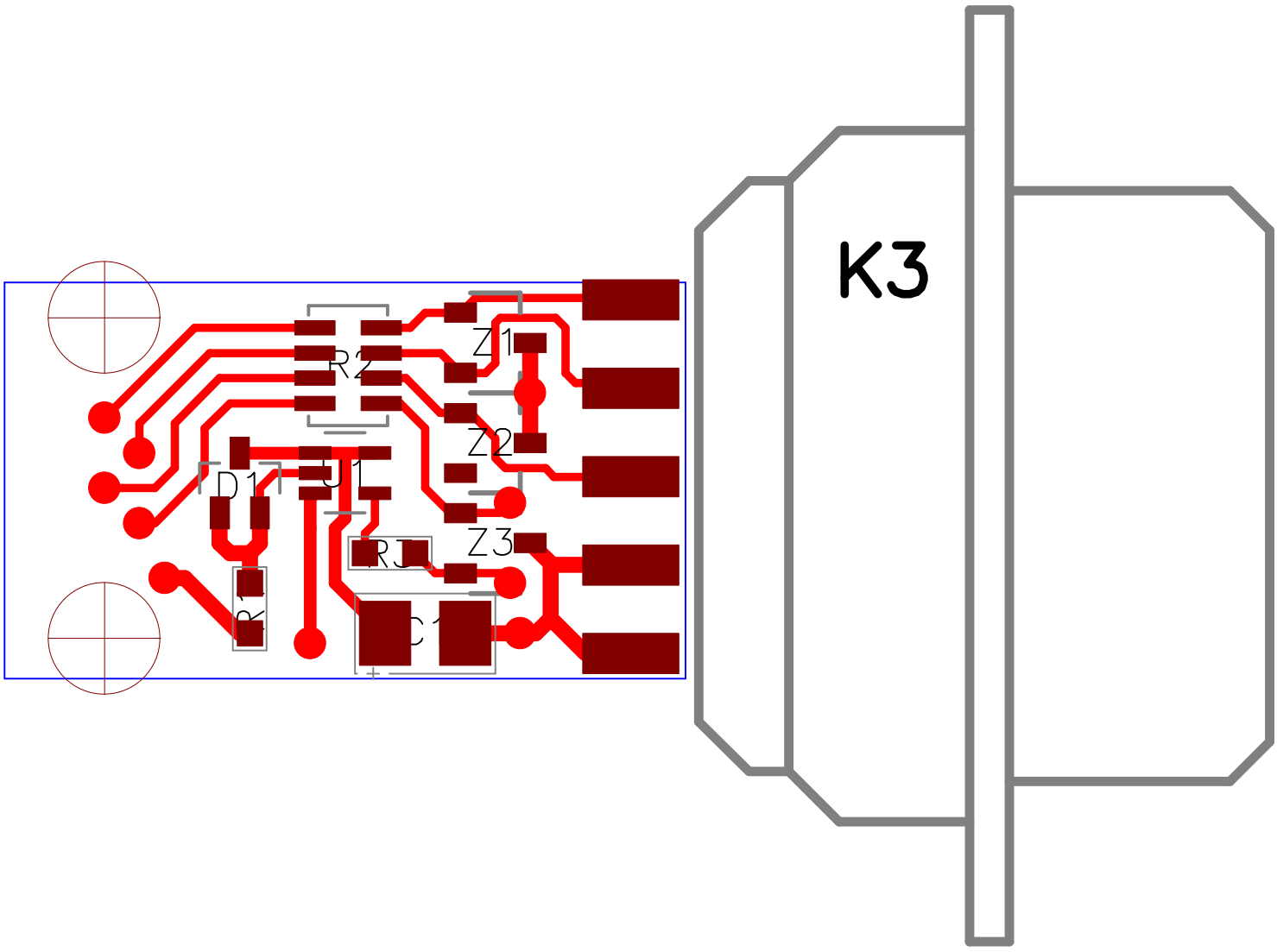
Mail me if you need any gerberfiles or additional info.
Don't fry your QL building this circuit! Good luck!

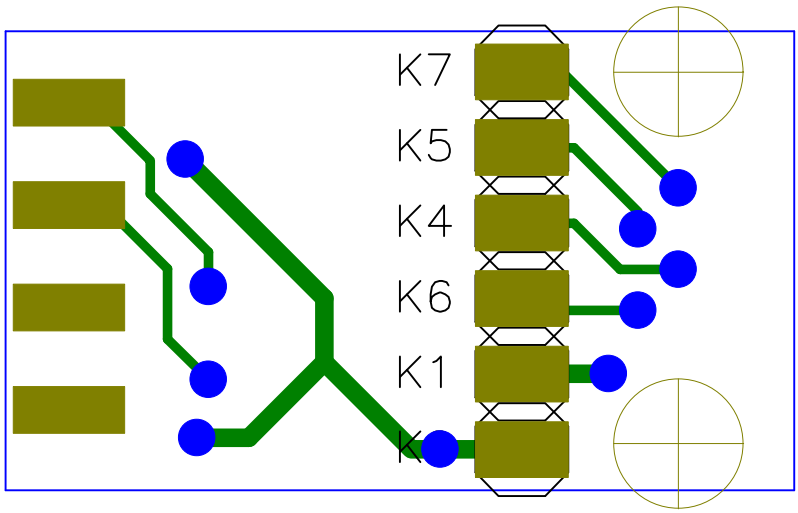
Marcel Flipse
mflipse**NOSPAM**@zonnet.nl

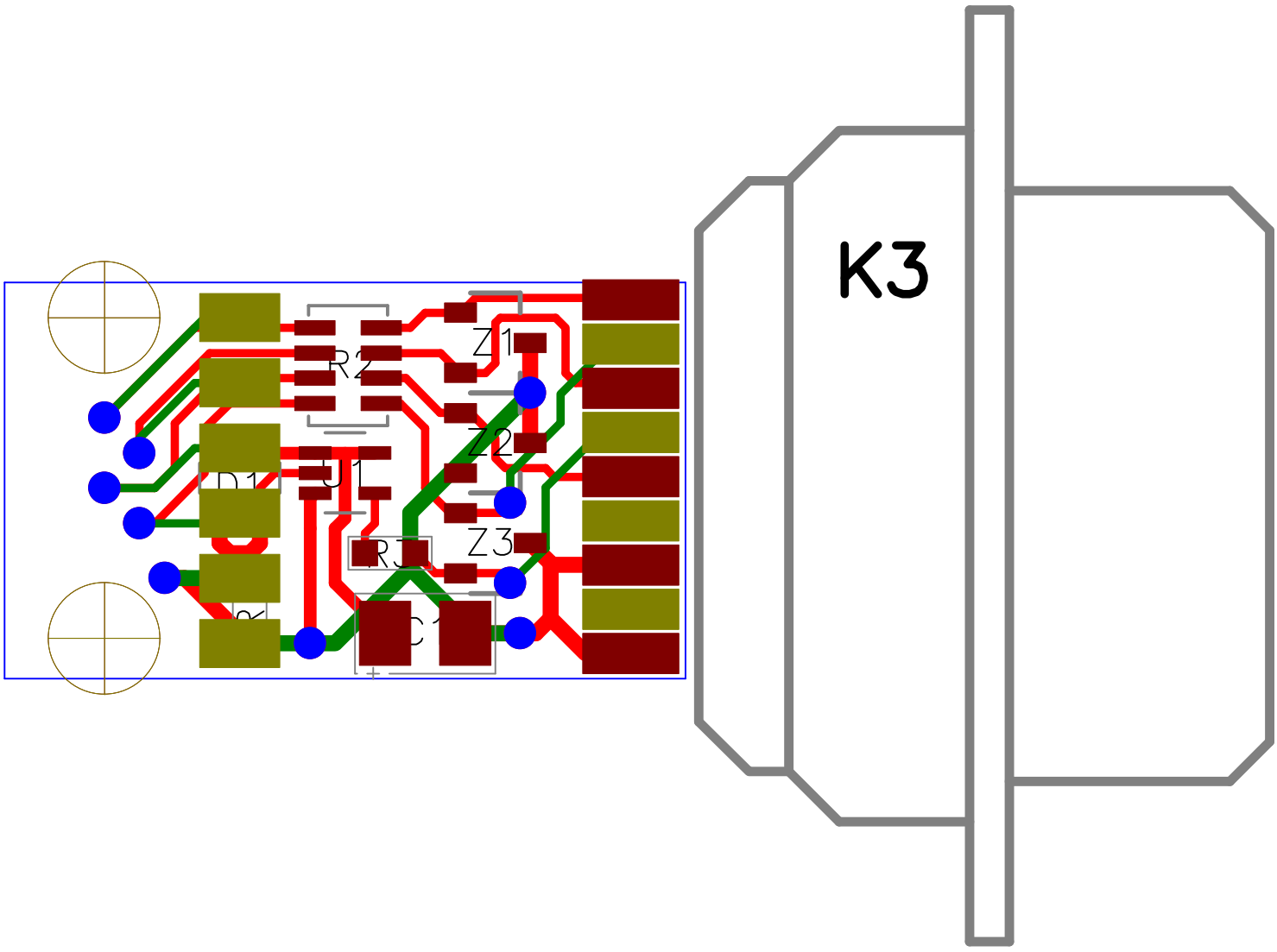


MIND DESIGN
Delftech Park
Elektronicaweg 25
2628 XG Delft
Tel: +31-(0)15-2131749
Fax: +31-(0)15-2131946
Eml: info@minddesign.nl

Title:	QL composite sync inverter		
Customer:	--	Rev:	1.0
Date:	Feb 2002	Drawn by:	M. Flipse
Filename:	QLsyncInverter.SCH	Sheet:	1 of 1


K3
R2
Z1
Z2
Z3
D1
C1


K7
K5
K4
K6
K1
K


K3
R2
Z1
Z2
Z3
D1