CST THOR PROFESSIONAL COMPUTER SYSTEM TECHNICAL MANUAL

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SECTION 1.00 QL Circuit Board Details

1.01. The CST THOR Professional Computer system is based on an under /populated version of the Sinclair QL personal computer circuit board. As several build levels of these exist, and the 'QL Technical manual' as published by Sinclair Research is generally inaccurate, it is intended to set out here an abbreviated description of the fundamental principles of operation of all versions likely to be encountered. It is assumed here that the ROM's or EPROM'S installed in the QL board are of the correct type for the national character set required by the user of the machine, and also capable of correctly linking in the extensions to the operating system of the machine which turn the QL into a THOR.

1.02. The QL design is based upon the Motorola MC68008-8 processor which uses 32-bit data registers and data paths internally, like the 68000,68010 and 68012 members of the same family. The 68008 however truncates the external range of memory addressing by using only 20 address bits compared to 24 on the other parts, giving a maximum range of one Megabyte. This has no direct effect on the performance of the processor, other than to limit the amount of contiguous memory which can be accessed. The data path however is only implemented as 8 bits wide, forcing the processor to perform sequential accesses to transfer words or long words of data or programme code. These sequential accesses are performed transparently by extra hardware on the 68008, which implements address line zero, to allow any single byte to be addressed. (This is done on the larger devices by decoding the upper and lower address strobe lines, which are replaced on the 68008 by a single address strobe). Naturally this type of sequential access has an effect on the overall speed of operation of the processor, and it is good programming technique to carry out as many operations as possible within the registers of the processor, using word length instructions, and keeping the number of long word accesses to a minimum. This has a direct bearing on the position of certain parts of the code within the system's memory-map, with the lowest 64K Bytes being specially valuable using the short addressing mode of the processor. At reset or power-on, the processor attempts to read two long words from the lowest addresses in the memory-map, these should contain the address of the restart entry point of the operating system code, and the address of a suitable memory location for use as the system stack, the next 254 long words are normally used for a table of addresses of the various service routines for Interrupts, trap calls, etc. For this reason this lowest IK of the memory-map is usually implemented in RAM to allow these vectors to be easily changed, however the QL design uses 48K of ROM starting at the bottom of the memory-map to simplify the address decoding, and this adds an extra level of indirection to the service code for all of these vectors, as they are pointing to fixed entry points in code elsewhere which then has perform a computed jump to the service routine required. This has an impact on the speed at which interrupts can be serviced, and in practice it is not possible to handle the double density floppy disc data rate by using interrupts or while they are enabled for system housekeeping purposes.

1.03. . The ZX8301 ULA controls the overall timing of the processor and video diplay. A 15 MHz clock oscillator is incorporated, which uses an external Quartz crystal to produce a stable reference frequency from which all other timing intervals are sub-divided. The maximum pixel rate of the video display is 10 MHz, and 512 pixels are displayed in 51.2 microseconds as the trace scans the face of the picture-tube. The timing is padded out to 64 microseconds per line to allow the scan to return to the left hand edge of the tube, and data for the next line of pixels is then transferred. 256 lines of pixels are transferred to complete a single picture, and the overall time for this operation is then also

padded out to allow the scanning beam to return to the top of the tube. The repetition rate for this entire picture is 50 Hz. In 4 colour mode each pixel is coloured according to the data contained in two bits of a byte transferred from memory, whilst in 8 colour mode 4 bits are used, reducing the number of pixels on a line to 256 for the same overall amount of memory (32 K) which is reserved for the video display.

The standard QL is fitted with 128K of RAM, which is made up of 16 64K x1 parts. The ZX8301 controls these on a private data-buss, which allows them to be read at regular intervals as required by the video display, but this imposes a penalty in the access timing allowed to the CPU. The 68000 processors use an asynchronous interface to the outside world, and this means that access cycles can be of variable length. In the case of the standard memory of the QL, the minimum length of an access is 533 nanoseconds, but due to the video display taking priority some cycles will take up to 1.6 microseconds to complete. This has a marked effect on the speed of operation of programmes, as all of the internal memory is affected in the same way although only a quarter of it is actually used by the video display. The hardware is arranged in this way to keep down the costs and to automatically refresh the dynamic memory devices as the video data is read out. Finally the ZX8301 generates interrupts to the processor at the end of every picture scan, in order that the task-sequencing code in the operating system can be controlled.

1.04. The ZX8302 ULA is intended to handle a number of functions, and has several registers which can be set up to allow control of these. Firstly, this component handles the timing of the system reset line, which is delayed for approximately a second after power is applied to the machine to ensure that the machine has been cycled enough times by the ZX8301 to be internally charged to a working state. Secondly a Crystal oscillator and binary counter is implemented, which counts in seconds to produce a readable clock for the machine. Third, the ZX8302 handles the outgoing data serialisation for the RS-232 ports, and the necessary handshaking inputs to control the sending process. Fourth, the ZX8302 controls the data serialisation and deserialisation of the network port (single line PNP open-collector pull-up type). Fifth, the ZX8302 controls the data transfers to and from the Microdrives, which are no longer implemented in the THOR machine. Fortunately removal of these devices fails-safe to the 'not found' condition as though no cartridge was inserted in the drive. Finally the ZX8302 handles serial data transfers to and from the 8049 Intelligent Peripheral Controller.

1.05. The IPC is a stand-alone mask-programmed microcontroller, which has it's own 11 MHz clock generator and ancilliary circuits to scan an 8 x 8 matrix of keyboard switches, two joystick ports (on the same matrix), control a 1 bit programmable noise generator, handle the incoming RS-232 lines asynchronously and buffer the data without disturbing the central processor, and communicate serially with the ZX8302. The keyboard scanning function is not used in the THOR, but without changing the masked code of this part, there is no way to actually disable this function without losing the RS-232 ports.

1.06. The Video outputs of the QL board are all based on the 3-bit RGB signals produced by the ZX8301. These are mixed with the synchronising signals to produce a composite monochrome signal with approximately 1 volt pk-pk data, sent direct to the monitor socket for a standard TTL input colour display, and also used to produce a modulated UHF signal without sound on channel 36 for a PAL standard television. Due to the bandwidth and picture convergence limitations of domestic televisions, a lower definition text mode is implemented for this situation, whilst monochrome and colour monitors should be able to display the high-resolution mode correctly. It is worth noting that most televisions and monitors expect a signal with only 40 to 48 microseconds of

displayable video per line, and that the correct setting for the QL would allow the entire transmitted 'test-card' to be seen on the screen with a small black border all round it.

Some televisions are designed to 'over-scan' to such a degree that it is not possible to reduce the width or height of the picture sufficiently to do this.

2.00. Startup sequence of standard QL.

2.01. The dynamic memory devices used in the QL design need to be cycled for a short period to build up their internal negative voltage supply before they will respond correctly to data-transfers. The Central processor unit also has a similar requirement, and to satisfy both of these needs, the reset and halt lines of the processor are held low for a period after the application of power to the machine.

The processor also requires this type of delay if it is reset without removal of the system power, and so the system reset button connects in through the ZX8302, which duplicates the timing of the power-on reset.

2.02. As the processor comes out of reset, it attempts to read the lowest two long words of the ROM, to find the correct address of the system stack area and the entry point address of the operating system code, if anything upsets this sequence, then the ZX8301 will display the contents of the video memory (which depends on the individual memory devices in the board) and the machine may then take many different actions depending on the exact nature of the fault. The most common symptom is that the processor cannot understand the data or op-codes which it reads, and enters a loop trying to run the buss error trap, which it may also fail to read correctly. Ultimately the processor may stop due to a double buss error, and this can be identified by examining the function code pins of the processor and the static values on the address and data pins.

2.03. If the restart vector is correctly read, the processor begins to execute the code at that address. This starts with a simple memory-test, which firstly checks the valid memory area at 64K intervals till it finds an address which does not give an alterable response. This is also affected by the non-use internally of the two most significant address lines from the processor, which limits the unexpanded hardware to a 256K memory-map. Subsequently the processor copies part of the lowest area of ROM into the RAM over and over again, until, the highest populated RAM address as previously defined is filled. This gives the familiar screen pattern, which is actually slightly different depending on the version of ROM installed. As the pattern is being written, it is checked, and any failure to match with the correct value results in the video display area being filled with a code which is displayed as a white screen. The processor at this point stays in a tight loop of code re-drawing this value onto the screen.

2.04. Once the pattern has been written, it is verified, starting once again from the lowest address. Any failure to agree with the contents of ROM during this part of the test causes the video display area to be filled with a code which actually produces a blank green screen, and likewise loops forever. Once the memory test is successfully completed, the code then sets up the Superbasic interpreter and tests for an expansion ROM in the slot at the rear of the QL. Should such a ROM be located, any banner message therein is displayed, and any extensions to 'Superbasic' or 'QDOS' are linked in. Following this, the main expansion area is similarily checked for additional ROM's, and if found, then any messages are diplayed and the code linked in.

2.05. Finally the remaining portion of the 'prompt screen' is drawn, allowing the user to decide which video format the machine is to be used in at that stage. The operating system then searches for a Microdrive cartridge in drive one, and if found, then searches for a file called 'boot' on that cartridge. If found, any 'Superbasic' programme in this file will be loaded and run, allowing the system to start up any desired sequence of operations, if no 'boot' file is found, then the next stage is simply to enable the command line interpreter and wait for input from the keyboard.

3.00 THOR hardware extensions to the QL.

3.01. The CST THOR professional computer system contains many extensions to the hardware of a standard QL. Most of these have been proved in previous products from CST, but they are now implemented in different ways to take advantage of the reduction in redundancy possible by making a combined unit. The THOR hardware is constructed on three printed circuit boards: a small vertical piece which has no active components, and serves both as a mechanical link to the QL,and a suitable place to apply the power to the unit; a second small board which mounts horizontally, and may carry up to six EPROM's, two of which contain CST's proprietary additions to QDOS; and the main circuit board, which carries all of the active components and the various connectors needed by the circuitry. Each major division of this circuit board is described below.

3.02. A Programmable Array Logic: device (PAL) is used to decode the system address lines, and generate the correct responses to the QL board whenever an access is made to areas outside the standard 256K memory-map. As the two most significant address lines of the processor are not connected on the QL main board, it is necessary to return a signal (referred to as DSMCL) to the QL to disable the ZX8301 whenever either of these address lines goes high. This is done by clamping the data strobe signal into the ZX8301 to the +5V rail using a transistor, and to avoid spurious effects, this must happen before the leading edge of the data strobe signal falls at the input to the ZX8301. A series resistor is fitted on the QL board to stop this clamp transistor holding the data strobe to other components high as well.

3.03. The THOR board has it's own buffered data-buss, and the LS245 buffer is enabled from the PAL at the correct times. This buss is damped with 150 ohm series resistors to limit transmission line effects. The remaining sections of the PAL are used in conjunction with an LS74 dual flip-flop and the processor clock signal to produce the timing signals for the 512K of Dynamic RAM installed on the THOR board. Two LS258 multiplexer devices are used to apply Al to A16 to the memory devices at the correct time, as row and column addresses. The memory is arranged in two banks of eight 256K x 1 devices, with alternate Bytes being addressed in alternate banks by feeding AO to the PAL to simplify the address decode. The memory devices used are of the more expensive CAS before RAS refresh type, which allow for the refresh of the memory to be completely transparent. The PAL generates a refresh cycle for the memory every time the data strobe from the processor goes active. Only during an actual memory access is the refresh stopped. This method actually increases the power consumption of the memory devices slightly compared to a distributed refresh system, but this was judged to be of minor importance- compared to the greater simplicity of the design.

3.04. Designed around the specification of the Alps Electronics 'IBM PC-AT compatible' keyboard, the serial keyboard interface is implemented with a Motorola MC 6850 device, which is connected to the data and clock lines of the keyboard in such a way that data coming in from the keyboard is self-clocking, but the THOR can generate a clock pulse locally to shift the start bit out onto the data line whenever data is to be sent back to the keyboard, which will

recognise the start bit on the data line and then generate the rest of the clock train. This process can go wrong when keyboard data is lost due to the keyboard being used during a data transfer to the floppy disc interface, when interrupts are disabled, and at these times, it is necessary to send a number of bytes to perform a reset at both ends of the keyboard cable. At present certain 'IBM compatible' keyboards do not respond to the software of the THOR, and it may be necessary to alter the code or even the hardware if there is sufficient demand for these types of keyboard in the future.

3.05. The parallel printer port is implemented using part of a Motorola MC6821 device. This is a dual 8-bit device, and data to be sent to the printer-port is written into the 'B' side output register. The hardware is decoded to allow an access to a specific address to generate a strobe pulse for the printer port, and the timing of this is decided by the same circuit, using an LS 113, which slows down the central processor to generate a '6800 peripheral' type of access cycle for both the 6850 and the 6821. An input on the 6821 is used to read the status of the printer's busy line, to sense the correct time for the transmission of the next byte of data. The interface is buffered with spare inverting elements from several devices on the board, and this means that data to be sent is actually inverted by the software before being written into the 6821 register.

3.06. The Mouse port is implemented using an LS74 flip-flop and part of the 'A' side of the 6821. Information from the mouse is applied to the LS74, which then gives outputs indicating the direction of movement, and a pulse train for each axis. This is easier to handle than simply reading the 4 lines from the mouse and having to make decisions about directions in software. Three buttons are also supported on the Mouse interface.

3.07. Two lines from the remaining part of the 'A' side of the 6821 are used to select drive 1 or two for the floppy disc interface, and these lines are 'OR'ed together as the Motor control line. The final two lines are used as side select, and double density enable, allowing the system to read single or double density discs from other systems.

3.08. The floppy disc interface is implemented using a western Digital WD1772 controller device, which has an internal digital data separator. It needs an external reference clock, and so an 8 MHz Crystal is used in a simple TTL oscillator to provide this, it is internally divided by the correct amount depending on the state of the double density enable pin. This interface is suitable for most 5 1/4" and 3 1/2" drives, but care should be taken that certain lines are not buffered and will not drive 150 Ohm terminating packs as fitted to many older drives.

3.09. The THOR system implements a battery-backed real-time clock, built around an Hitachi HD146818 device. This operates with a very low-powered crystal oscillator running at 32768 Hz, and will continue to operate for at least 14 days when the system is turned off. Operating from a re-chargeable 3.6V Ni-Cad battery, which is trickle-charged while the system is in use. To avoid upsetting the clock, a transistor is used to control the system's access during the power-up period. An input to the clock device senses the supply voltage, and when the battery is completely discharged this sets an internal flag at power-up, which is used to warn the system that the clock may not be accurate.

SECTION 4.00 THOR startup sequence

4.01. Initially the power-on startup sequence of the THOR system is identical to that of the standard QL computer, on which it is based. Once the sequence reaches the point described in section 2.04., where additional ROM's are searched for, instead of allowing the sequence to proceed as before, the user

ROM area is checked at 16 K boundaries for the presence of additional ROM's, until the first THOR ROM is located. This contains code which sets up the hardware of the THOR circuit board, but then it modifies the contents of the registers used in the search routine, such that the last three 16 K blocks are not accessed. This is done to prevent there being any uncontrolled accesses to the hardware area of the THOR board, which is transparently accessed as 'data space' at the same physical addresses as the highest ROM slot.

4.02. THOR ROM's from issue 4.00 onwards contain both a checksum verification routine, which should guarantee the integrity of the code therein; and a serial number/watermark identifying the machine as a THOR. This can only be checked by using a new trap-call in the extensions to the operating system. No attempt should be made to verify this by direct access to the ROM's as any access to this area will cause a hardware lock-up of the machine to occur.

4.03. The code contained in the initialisation sequence of the THOR ROM 's sets up the different components on the board in a specific sequence. This sequence is of necessity complex because a number of the components are inter-dependant. In particular, a number of sections of the circuitry are capable of generating interrupts at certain times and these must not be enabled before the requisite service routines have been linked in to QDOS.

The Floppy disc system needs the undivided attention of the main processor during reads and writes, and therefore all interrupts are masked during disc accesses. During the startup sequence, the operating system performs a test to find the maximum stepping rate which the floppy drives wil1 handle, and then tries to copy the directory of the first drive into memory, and searches for a 'boot' file. Until it is satisfied that none is present, the flashing cursor on the input line of the screen will not appear due to the system's temporary inability to handle interrupts from the keyboard. The cursor also disappears during subsequent disc accesses for the same reason. (Unlike the standard QL, the keyboard is not handled by a co-processor, and any keystrokes made during this period will be lost).

In single disc systems, a second drive is always checked for, and this check times out slowly due to the

non-detection or the index pulses from the second drive. If two drives are fitted, and neither has a disc installed, then this time delay is similar for each drive in turn. The quickest exit from this test is if both drives have a disc-installed, but neither has a 'boot' file present. At this point the default device is changed to FLP1_.

4.04. The code then tests for the presence of the SCSI interface circuitry, and if it is installed, regardless of the presence of the actual Winchester drive, the default device is set to WIN1_. This is carried out after the tests of the floppy disc system, in order that a system with a corrupted Winchester 'boot' file can be diverted by inserting a floppy disc which itself contains a valid 'boot'.

The sequence is designed to allow the correct initialisation of the system with a new (unformatted) Winchester drive, and it is not recommended that the system should be operated with the SCSI components installed, but without the actual drive. This does not cause any damage, just confusion over defaults. If the Winchester is present, and correctly formatted, then the directory is copied into memory in the same way as for the floppy disc.

Certain operations may seem to take longer on the Winchester disc, and this is due to the directory mechanism used. 16 K of memory is used for each directory present on the device, and due to the pre-sorting algorithm used when making directory entries, the full 16 K is scanned even if there is only a single

entry. The SCSI data transfers are handled using interrupts, and this makes Winchester accesses interleave with other interrupting events. Typically the keyboard will be useable during Winchester accesses. The Winchester system also performs 'write behind' to minimise the number of seeks made to the disc and this should be remembered when powering down the system, as the transfer of files may not be completed for a number of seconds.

4.05. The real-time clock is read during this sequence, and if the system has been powered-down for some length of time, then the message 'the clock has been reset' will be displayed on the screen. This is a warning that the date and time of the QL's clock will not have been set from the battery-backed one, and 'sdate' followed by 'set_clock' should be used as detailed in the owner's manual. Under normal, circumstances, the QL's clock will be set to the same date and time as the battery_backed unit, and no warning message will appear.

4.06. The keyboard interface is enabled at this point, and this works by forcing the values of any keystrokes into the buffer previously used by the 8049 processor of the QL. This is done for compatibility with existing software, as

certain applications packages, and the 'alt-enter' keystroke sequence (restore previous line) directly read from this buffer.

4.07. Once the type of storage devices present has been identified, the code re-joins the standard QL power-up sequence, and performs an 'Irun' comrend on the 'boot' file if found on the default device.

5.00. optional SCSI Interface.

5.01. The THOR computer system has provision for a Small Computer Systems Interface (SCSI) port to be installed on the main circuit-board. This hardware is able to interface to SCSI devices using the 'single master' system, no provision is made for bus arbitration between intelligent peripheral devices to take place.

5.02. The SCSI standard defines voltage levels, pin connections, and minimum timings of all signals used by the interface circuitry. However, the system is asynchronous in operation, with no maximum time limits being imposed on many of the operations of the interface. The highest speed of data transfer using this type of interface requires DMA hardware, but this is not implemented on the THOR.

5.03. The hardware consists of 4 Integrated circuits which may be field-installed into sockets provided on the circuit-board. Several passive components are also required, but it has been decided that these will be incorporated into the assembly of all issues of the circuit-board at the factory, to avoid the need to remove the circuit-board from the chassis during conversion.

5.04. The Components required for the SCSI interface are IC.11 (74LS05) a hex open collector inverting buffer; IC.12 (74ALS638) an inverting octal tri-state line driver/receiver; IC.13 (PAL 16 L8) a programmable logic device with proprietary design to control the interface timing; and IC.15 (74LS245) an octal bidirectional three-state line driver. These parts will be available in the THOR spares kit from CST.

5.05. The SCSI standard also defines the 'Common Command Set' or CCS, which is a small kernel of the possible instruction codes available. This is intended to persuade different peripheral manufacturers to use the same group of commands uniformly, to allow a greater degree of interchangeability between their products. However at present this is not the case with 20 Megabyte Winchester discs, and the THOR software presently supports only the RODIME R0652 drive.

The driver software has presently been left so that up to eight devices can be addressed, however they must all be the same type. It is possible that the code in later issues of the THOR ROM's will be extended to allow the use of other specific devices on this interface.

5.06. The SCSI interface as implemented on the THOR computer is normally connected to an internal device, powered from the internal voltage supplies. However access has been provided to the connector through a slot at the top

of the rear panel of the machine, so that externally powered devices can be connected. If this is done, it is necessary to arrange that only the devices on the ends of the ribbon cable are fitted with terminating resistor networks, and that the device on one end is no more than 150 mm away from the connector on the main circuit-board. The interface uses the single_ended signal convention, and there is therefore a 1imit of 3 Metres maximum between the first and last devices on the cable. Devices should all be of this type; balanced line devices will not work.

5.07. The Winchester disc is formatted in blocks of the standard QL size (512 bytes), and block transfers are initiated by interrupts from the interface circuitry. However these block transfers are interruptable, and therefore other operations can proceed while data is transparently transferred at a slightly reduced speed. This compares favourably with the floppy disc interface, which has to mask all interrupts and poll the disc controller device continually during data-transfers.

SECTION 6.00. Hardware upgrades.

6.01. The basic production specification of the THOR computer system includes a single 3 1/2" 80 track double sided double density floppy disc as the data storage device. This can be supplemented by the addition of a second identical drive, a second non-identical drive (if required for media compatibility with other systems), or by fitting the SCSI interface components and a 20 Megabyte 3 1/2" Winchester drive.

6.02. Access to the internal components of the THOR system is obtained by removing the four M3 screws which secure the top cover, and then sliding this cover forwards until it is free of the chassis. This may be made easier if three of the four screws securing the plastic feet of the machine arc slackened first. The screw holding the rear left-hand foot should not be slackened, as it is used internally to secure the main printed-circuit-board to the chassis.

6.03. The standard assembly arrangement is that single floppy versions of the system have the drive (selected as drive 1) installed in the rightmost slot of the chassis so that when a Winchester drive is installed, it will be fitted into the central position.

When a second floppy drive is installed, placing it into the central position in the chassis would make the logical sequence of drive-numbering incorrect, and it is recommended that either the original drive is moved to the central position, with the new drive (selected as drive 2) installed at the right-hand side, or that the selection links on both drives are adjusted to place drive 1 in the central position.

6.04. The exact details of this link-adjustment procedure vary from one make of drive to another, so it may be necessary to consult the drive manufacturer's information to carry this out correctly. In most cases, there will be a double row of small pins sticking up from the surface of the circuit-board of the drive, and there will be one or more push-on bridging plugs already installed on

these pins. It is likely that a legend will be present on the circuit-board, with DSO, DS1, DS2, DS3, and possibly HM, HS, DS, or MX markings. The THOR software uses drive 1 and 2 to identify the devices, but the actual drives use DSO for drive 1, and DS1 for drive 2.

Install the bridging plug across the correct pair of pins before installing the drivers). The other selections are less important, as they will only affect the internal time-delays of the drive during the selection process. The THOR software should cope with any setting you are likely to

encounter. If you have problems, refer to the drive manufacturer's data-sheet.

6.06. Certain drives have their interface circuitry built with C-MOS devices to reduce power consumption for portable computer systems; the THOR circuitry may not operate correctly with this type of drive, especially if a mixture of drives is installed in the machine, it may also be desired to extend the connections outside the THOR case to connect to existing drives (possibly 5 1/4"), and it must be made clear that this will only operate correctly if the length of the cable is kept down to less than 1 Metre, and the drives do not have terminating resistors fitted.

6.07. All machines are shipped with a power cable for two floppy drives installed, it is necessary to replace this with the alternative part for the Winchester upgrade. These cables use insulation displacement connectors, and care must be taken not to loosen the wires as they are handled. These cables are all fitted in identical positions, and the only difficulty likely to be encountered is the removal of the connector from the small vertical circuit-board, which has locking clips behind it. This may be made easier if the QL circuit-board is removed first (3 screws), to improve access.

6.08. Single floppy machines are shipped with a ribbon cable with only two connectors installed. It is necessary to replace this with a three-connector version for the dual floppy machines, or to add the Winchester cable for SCSI machines. These cables are fitted by pushing the connectors on to pins on the drives and on the main circuit-board, and polarity is important. The dual floppy cable has an identical section to the single floppy cable, and this should be installed in the same position. The additional connector can then be fitted to the second drive, with the connector the same way round as that on the first drive. The Winchester cable will only fit one way round, as there are different numbers of pins on the two connectors. It is important to check that there is not a twist in the cable, as this will stop the system completing the power-on reset sequence.

6.09. All necessary hardware (bolts, spacers, cables, etc) will be provided in upgrade kits supplied by CST, and installation instructions will also be provided where necessary.

It seems likely that a number of dealers will want to carry out their own upgrades, and with this in mind full details of the parts needed are included in the main parts-list at the rear of this manual. CST will not accept liability for any consequential loss or damage caused by the installation of dealer-supplied upgrades to the THOR system.

certain items will only be available from CST, or their agents, most notable of these is the Winchester upgrade kit, which includes the Custom PAL device for the SCSI interface. The price of these components also inherently includes a licence fee for the use of the proprietary SCSI interface drivers provided in the THOR ROM's, and the Winchester utilities disc which will be shipped with this kit.

6.10. The upgraded THOR system should be given a full functional test, including the formatting of a Winchester drive if installed. CST has test software available to dealers to simplify this process, but it is preferable that this test is carried out before the cover is re-fitted, and then repeated after several hours of running with the cover installed. The power-supply of the THOR system is specified for the fully_upgraded system; however the power consumption is doubled when the Winchester drive is installed, and this will result in a higher operating temperature than systems which only have floppy drives. This increase in temperature may show up faults which have previously gone unnoticed.

7.00. Test and maintenance of the THOR system.

7.01 The THOR professional computer system is based on the main circuit-board of the Sinclair QL computer, with numerous additions to both hardware and software. As the QL circuit-board is mostly unchanged (issues 5 to 7 with JS ROM's), it can be tested in isolation from the remaining components of the THOR. It is only necessary to provide the board with a regulated 5 Volt supply, and a standard QL membrane keyboard in order that the normal QL test procedures can be carried out.

If necessary, Microdrives can be used to assist in the rapid loading of test software, but unmodified microdrives will not function if connected, as they require an unregulated 9 Volt supply. The THOR system uses the old 9 Volt output pins of the expansion connector to feed its 5 Volt supply on to the circuit-board, and the 9 Volt and 5 Volt traces on the board are connected together. Microdrives can be modified to operate with this 5 Volt supply by removing their 7805 voltage regulators and linking the two outer pin-positions together on the board.

If no other means of powering the QL circuit-board is available, it is possible to make an adapter which transfers power from the THOR chassis to the QL board via a backplane type DIN 64-way connector on flying leads.

7.02. The QL circuit-board contains several custom logic devices, and a mask-programmed microcontroller. Two of these devices are generally the most likely components to cause problems with an established QL board. The Video Controller device (ZX 8301) is easily damaged by outside influences, as it drives the RGB video monitor directly. If the video monitor used is not separately grounded, and is then plugged into the THOR system whilst still carrying a static charge, the device will very often be damaged as the static will discharge through whichever pin makes contact first. The output drivers of the device are only specified against temporary short-circuits to ground or the 5 Volt supply, and as little as 10 Volts will cause permanent damage.

7.03. Symptoms vary, depending on the exact damage done to this part. In general the system will power-up with a blank white screen, with or without synchronising pulses for the monitor, but there are also failure modes where the screen carries a fixed pattern, or one or more colours fail to appear. Normally when a blank white screen appears, the system never comes out of reset, as the white screen is an indication of total RAM failure. This is not totally surprising, as the RAM timing is controlled by the Video Controller, and the reset sequence tests all RAM before

doing anything else. The modes with a pattern displayed on the screen are usually due to internal short-circuits between address lines inside the Video Controller (a similar situation arises when an external short is present in the machine), but the timing chain is still intact. The display represents the power-on state of the memory devices in the video display area, which the processor is unable to set to white due to the address-line fault. Missing

colours are simpler to diagnose, as the rest of the system still works correctly.

7.04. The ZX8302 communications controller is also prone to failure due to the number of connections which are brought out to the outside world. Firstly the external interrupt line of the expansion connector is fed directly to this device, and unfortunately it is on the pin next to the -12 Volt supply. A bent pin on the expansion connector is all that is needed to destroy this device, and although this should not happen internal to the THOR machine, it can still happen to the connector in the expansion slot at the rear. A variety of symptoms can follow from damage to this component, with the most common being the sudden 'slowing down' of certain machine functions due to the overhead involved in servicing a permanent but unidentifiable interrupt.

Other lines on this device which appear externally are the handshake lines of the serial ports, and again a wide variety of faults can occur as a result of damage to this component. Failure to transmit to a serial device, 'not found' messages when the device is actually ready, etc.

7.05. Naturally over a period of service, there are many things which can cause problems with a system as relatively complex as the QL circuit-board, however, fortunately there seems to be a relatively low failure rate on the major components used, apart from the situations described above. The Central processor device (MC68008-8) is prone to damage from external hardware, especially when it is remembered that all of the address and data lines of the system originate from this part, and are all unbuffered at least as far as the expansion connector. The THOR hardware does buffer the data lines, but they represent only a small group, and it is likely that they will also be unbuffered on any add-on card.

Peripherals should always be connected when the system power is switched off, and wherever practical all elements of the system should be independently earthed to remove the risk of damage from static charges. Always use a good mains distribution block, and make sure that the mains leads are the FIRST thing which you plug in when setting up the system. This guarantees that any static charge will dissipate safely through the earth wiring, and. that there will be zero potential difference between items which are to be connected

together.

7.06. Memory faults on the QL are of two kinds; firstly, there are those which are induced by the Video Controller device, when it is itself faulty; secondly there are genuine memory device failures. The first category are easily solved, as they disappear when the Video Controller device is replaced. The second type are more difficult to trace, in general the more catastrophic the fault, the easier it is to locate. It sometimes helps to hold the QL reset button in when powering up the board, as the pattern then displayed is the natural reset state of the memory devices.

Thin vertical lines on the screen at regular intervals can indicate specific bits faulty in the RAM, but further diagnosis is assisted by the QL's memory test sequence, which stays in a loop of code, writing a known value to the screen memory at successive locations when it fails. It is necessary to investigate the individual memory devices using an oscilloscope, to search for unusual waveforms.

7.07. Further investigation of the QL board is likely to be a lengthy business, with intermittent faults being particularly difficult to locate. Without test firmware in ROM, a digital storage 'scope, or a logic analyzer, it will often be simpler to obtain a service-exchange replacement for the QL circuit-board. If you return a faulty board under these circumstances, please give as full a

description as possible of the problem, as it may not re-appear immediately when the board is being repaired by CST.

7.08. The THOR main board is currently built using a relatively large number of discrete devices, as this was judged to be the most economical method for production quantities below 1000 per month. The largest category of faults encountered so far is due to the low-volume hand-assembly techniques used, and due to the stringent quality-control checks, these rarely leave the factory uncorrected.

There is presently insufficient data to suggest that any specific failure pattern has occurred in the field. Whilst this is reassuring in general terms, it has the unfortunate side-effect that every fault is likely to be a new one, and therefore all the more difficult to track down.

7.09. The larger integrated circuits, and the custom PAL devices are all installed in sockets to reduce the chances of damage from static charges while the boards are being handled in the factory. There is no reason to suppose that they are more likely to fail than the other components, and they should not be removed from their sockets without proper anti-static precautions being taken. It is

occasionally found that atmospheric pollutants can cause problems with the sockets, but careful removal and re-insertion of the components would seem to be a sufficiently good method of removing any surface contamination. Spray-cleaners should not be used, as they often leave an oily residue on the surface of the circuit-board. This can become a sticky mess with small bits of dust and dirt mixed in over a period of time, and the added capacitance of such a deposit has been known to upset the operation of computer systems.

7.10. The THOR hardware can fail in a variety of ways, but in general it is unlikely that any of these will stop the QL board from operating normally. Memory faults can stop the power-on sequence being completed, but applying a temporary ground to pin 9 of 1C 4 the main PAL device, will disable the THOR's RAM completely. If this allows the power-on sequence to complete (with 128 K of RAM), then a memory test can be carried out from superBASIC, with the ground removed, to locate the problem.

7.11 Generally it will be found that the circuitry used on the THOR main board is sufficiently modular that specific faults can be rapidly diagnosed within the small area of circuitry associated with particular functions. However, there are faults which can cause the THOR hardware to stop the QL board operating correctly, and among these the most likely is for a faulty component to either short two signals together internally, or to ignore an input. Both of these conditions are likely to stop the power-on sequence at some indeterminate point, and without the use of an oscilloscope or logic-analyzer to examine the state of all relevant signals at the central processor, it is very difficult to make an accurate diagnosis. Typically a processor cycle will start by placing a valid address on its outputs, and then activating the address and data strobe lines (active low). If the address is in THOR board space, then IC4 the main PAL should take pin 14 high, activating the DSMCL line via Q1. Pins 12 and 13 should be in the appropriate state for the actual address present, and either DTACK or VPA should be activated to complete the cycle. Usually neither of these signals will occur, holding the processor from completing the cycle. Depending on the specific address, the state of the logic chain can be followed until the reason for this inactivity is located.

7.12 The second class of fault likely to be encountered is that which does not complete the power-on sequence, but which appears to be executing code. Again the exact hardware state must be checked, but when DSMCL, DTACK, and all address and data lines appear to have normal signal levels on them, it is likely that

one of the peripheral devices is not returning the expected value when polled, and the processor is running a loop of code which is waiting for

the correct state to occur. The chip-select inputs of the various devices can be examined to find the one primarily involved, and other inputs to that device can be examined to locate any unusual signal conditions.

Alternatively, it is likely that at least one of the processor pins will show an unusual signal level, and it may be necessary to follow the tracks on the circuit-board to locate the reason for this irregularity. Bear in mind that the RAM has its own local data buffer, and that a short between lines on the RAM side of this will just look like identical data on two lines at the processor. Equally, the read/write line is buffered independently for the RAM and all other devices. The signal may be present at the CPU, but not at the RAM or the other devices.

7.13. The RAM array has its local address lines multiplexed in IC's 16 and 17, and it may not be obvious that the address lines may be perfectly alright at the processor, but shorted together, open-circuit between memory devices, or not being multiplexed at all. In normal operation, the main PAL device outputs two types of timing pulses on pins 16, 17, 18, and 19, to control the RAM during normal access cycles and refresh only cycles. It may be worth disabling the RAM as described in section 7.10., to stabilise these signals to the refresh only type when searching for a RAM fault.